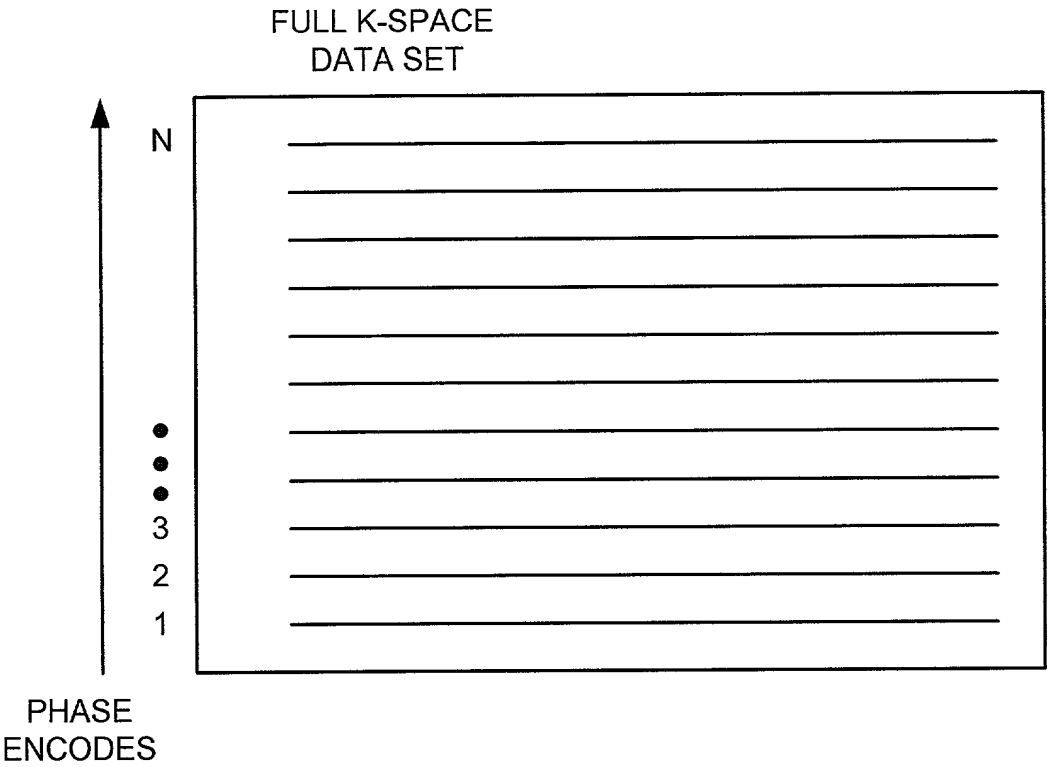


FIG. 1



NON-INTERLEAVED
ORDER

FIG. 2A

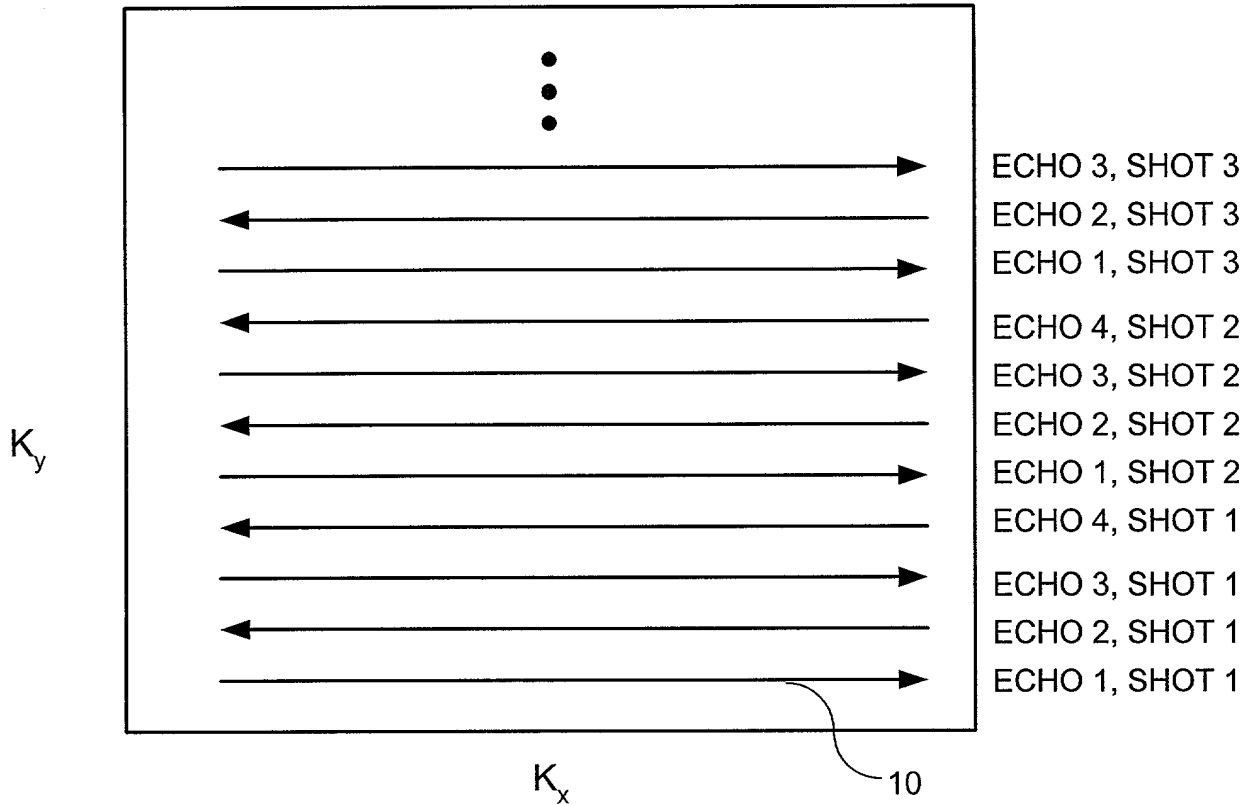


FIG. 2B

INTERLEAVED ORDER

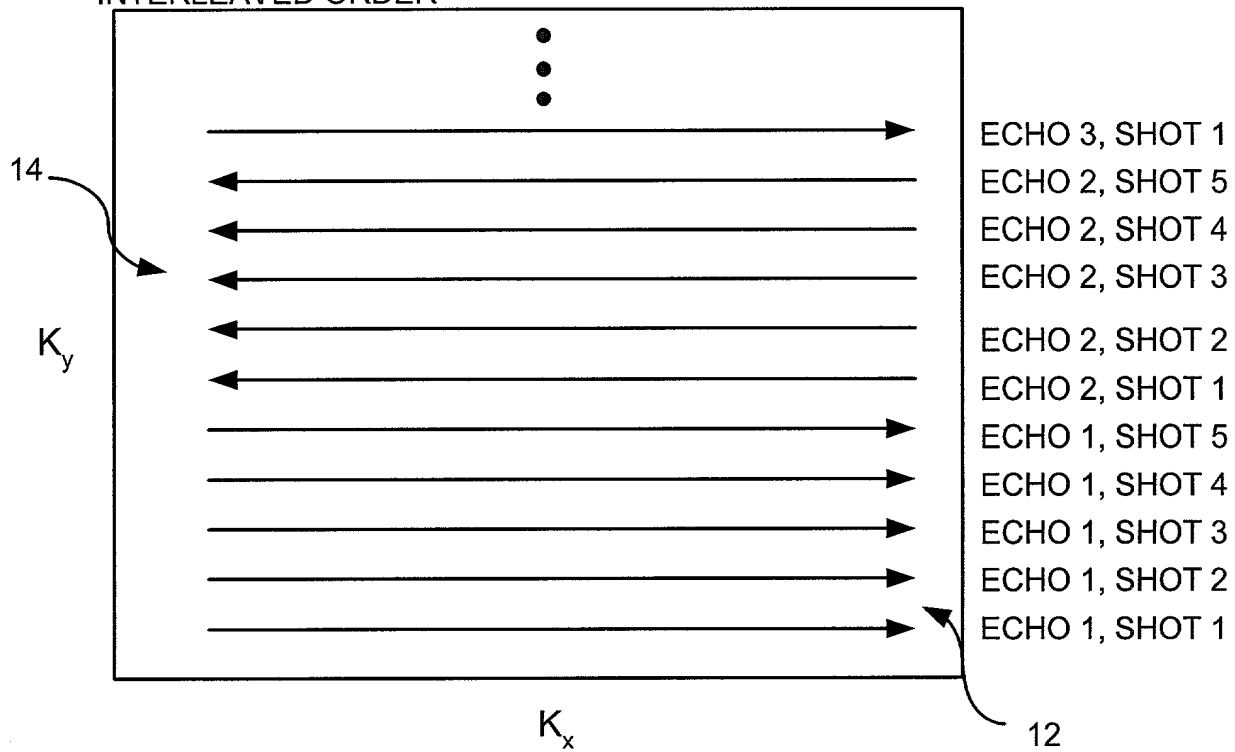


FIG. 3

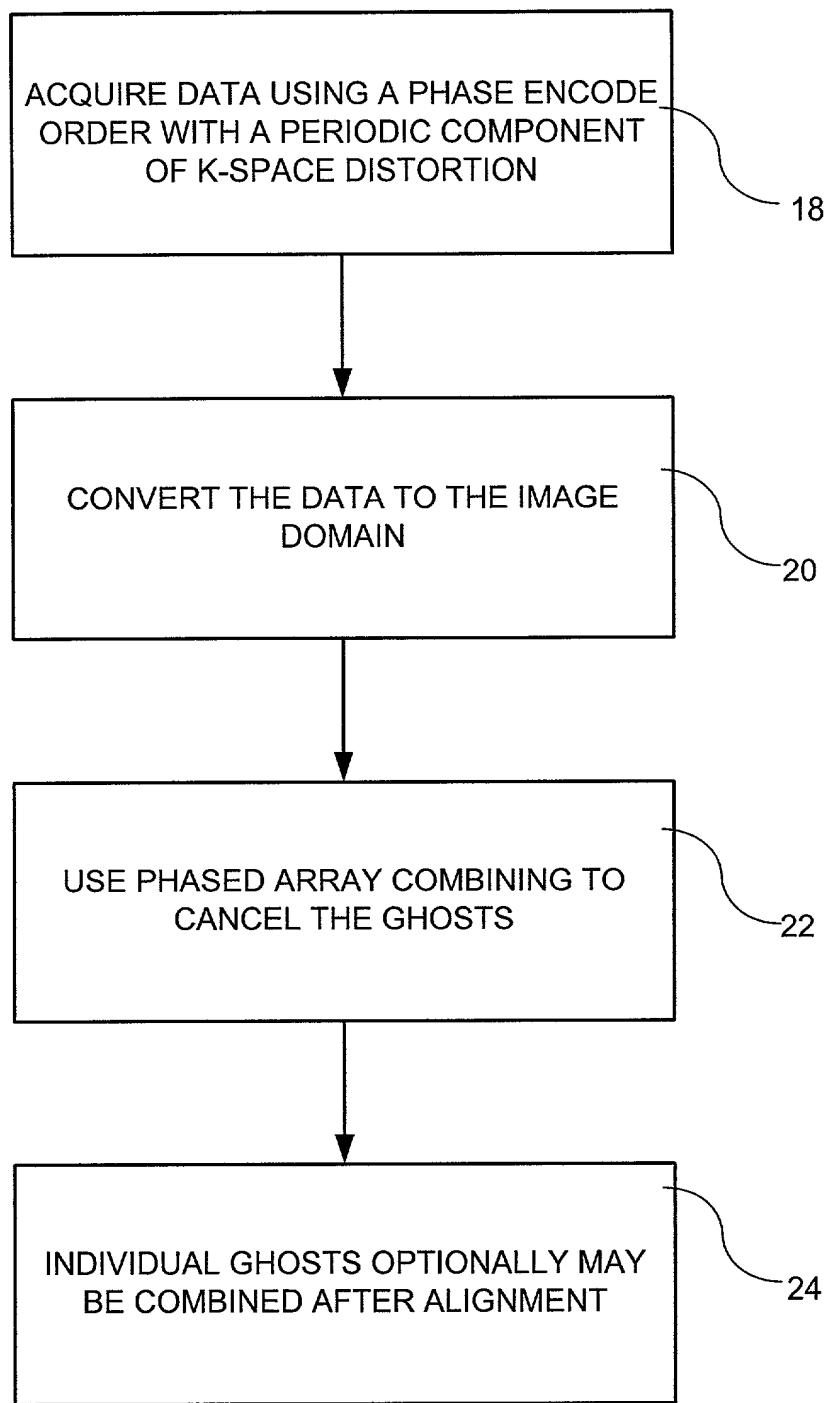


FIG. 4 is a block diagram of a multi-coil k-space data processing system. The system includes a multi-coil k-space acquisition block (29) that outputs multi-coil k-space data (30). This data is processed by a converter to image domain block (30). The output of the converter is then fed into two parallel processing paths. The top path includes an array combiner block (34). The bottom path includes a shift block (38) followed by an array combiner block (36). The outputs of both array combiners are then combined by a combiner block (40) to produce the final output (32). The entire processing path from the converter to the final output is enclosed in a dashed box (28).

FIG. 4

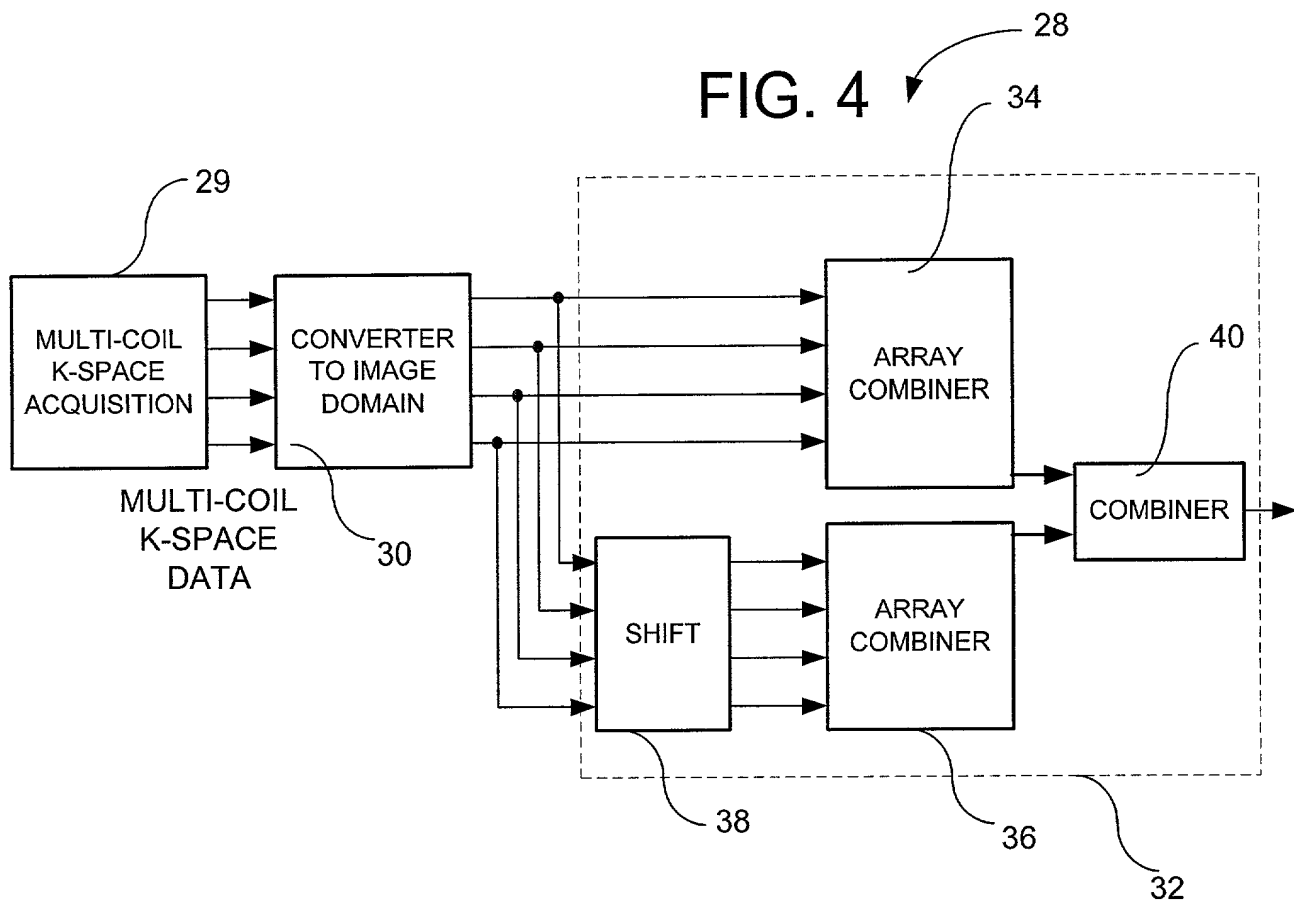


FIG. 5

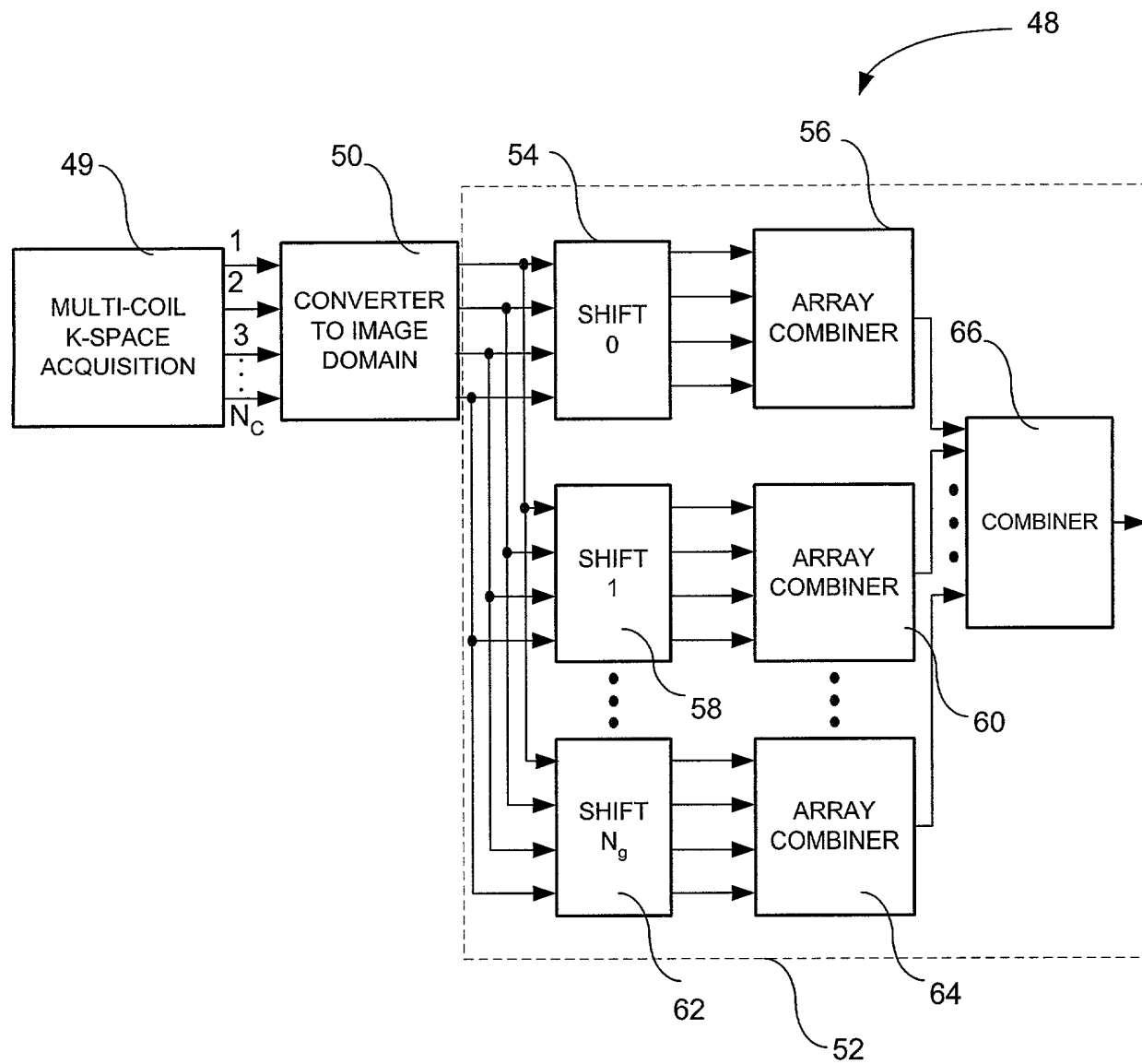


FIG. 6

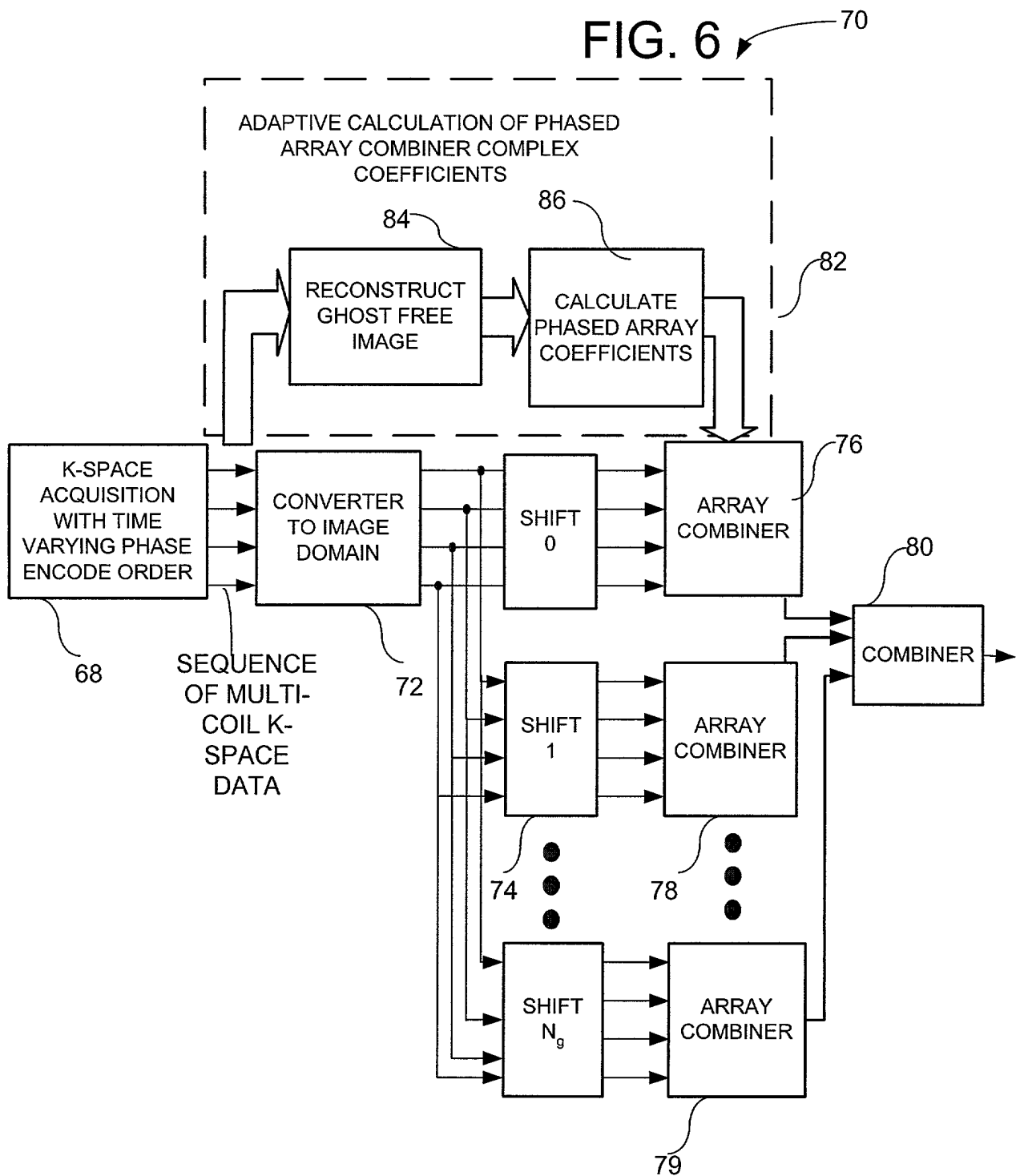


FIG. 7

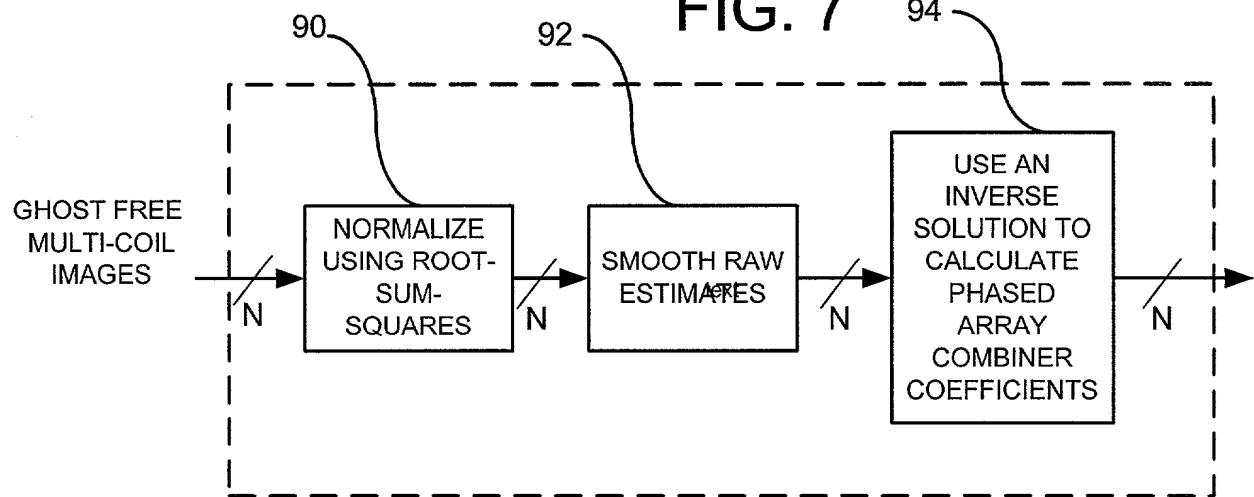


FIG. 8

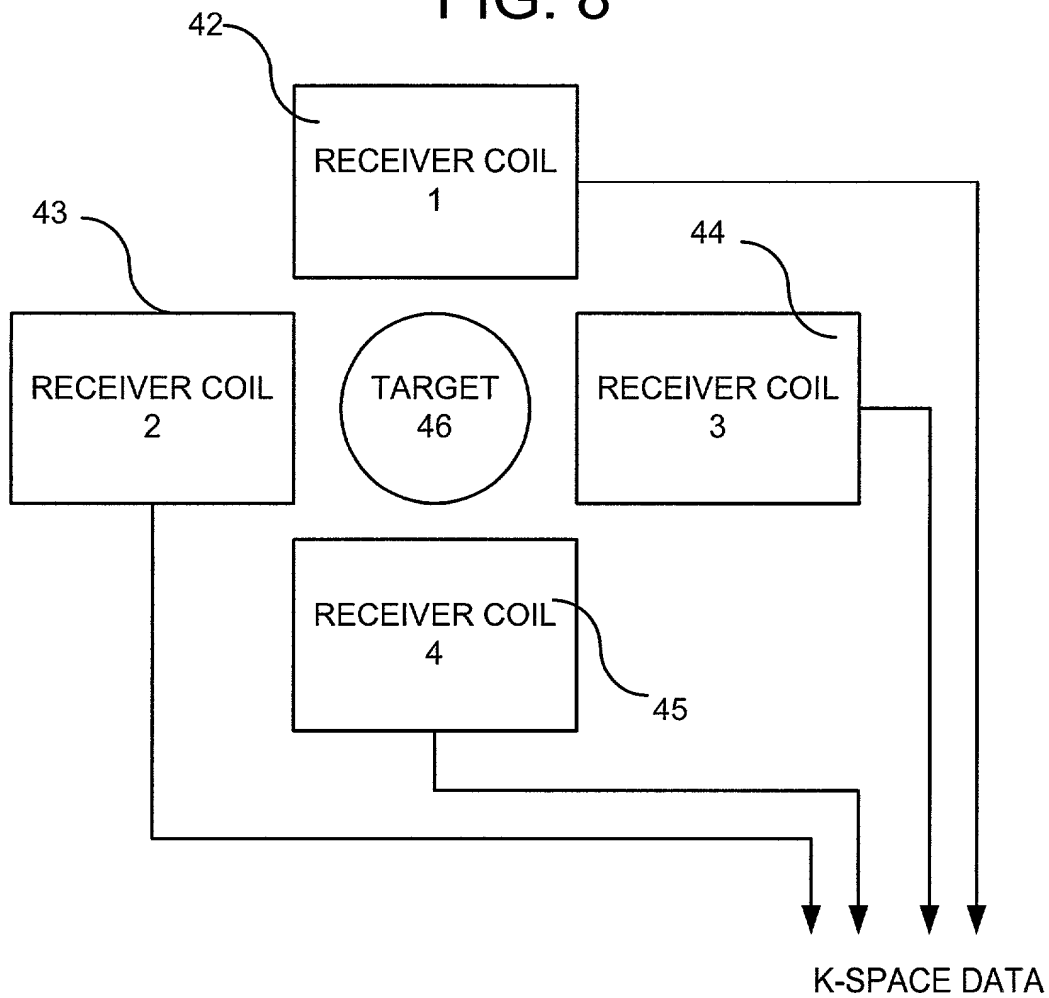


FIG. 9A

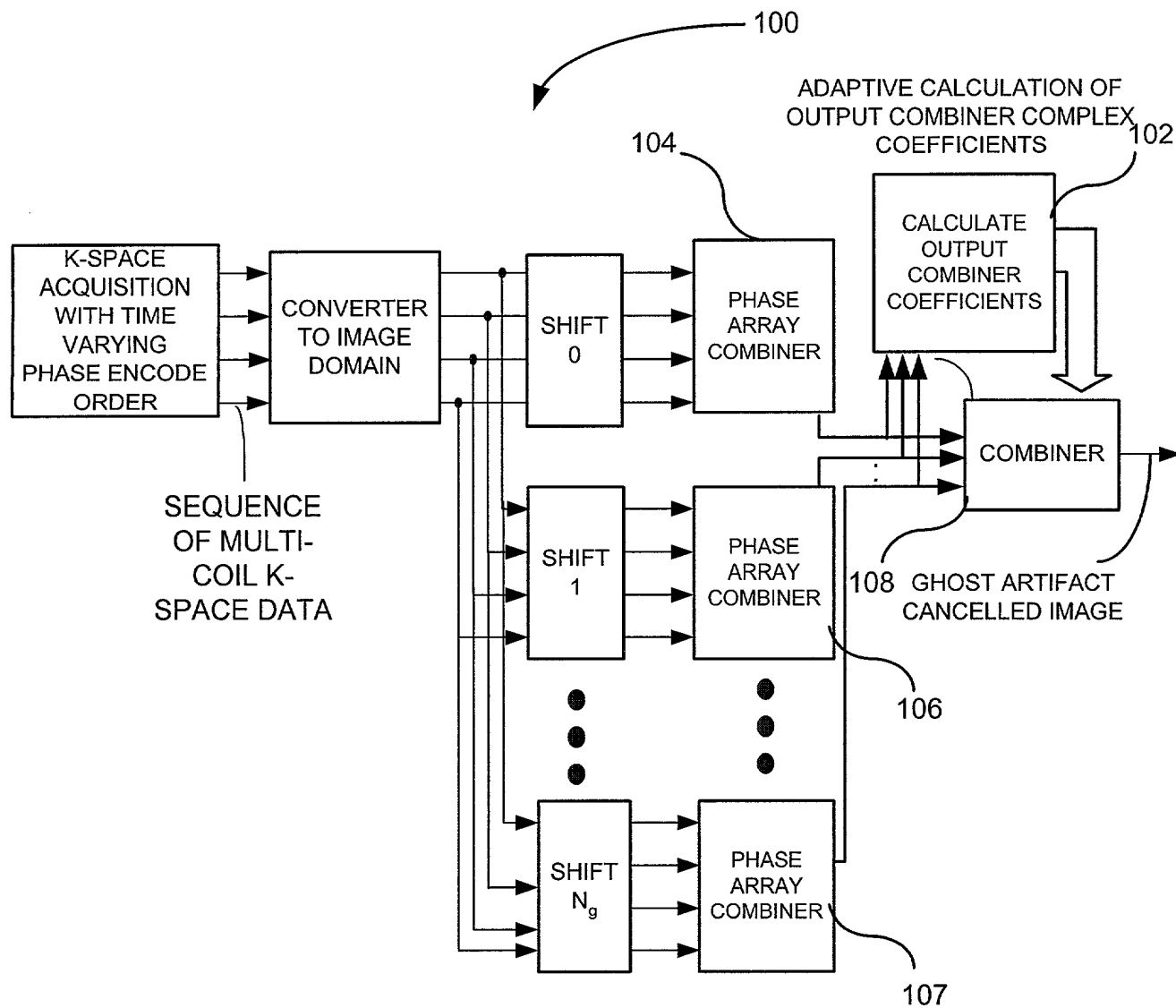


FIG. 9B

